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# Fast-Response Load Regulation of DC-DC Converter By High-Current Clamp

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## ABSTRACT

A new fast-response high-current clamp DC-DC converter circuit design is presented that will meet the requirements and features of the new generation of microprocessors and digital systems The clamp in the proposed converter amplifies the current in case of severe load changes and is able to produce high slew rate of output current and capability to keep constant the output voltage This proposed high-current clamp technique is theoretically loss less, low cost and easy to implement with simple control scheme. This is modified from a basic buck topology by replacing the output inductor with two magnetically coupled inductors. Inductors are difference in inductance, one has large inductance and other has small inductance The inductor with small inductance will take over the output inductor during fast load transient It speedup the output current slew rate and reduce the output voltage drop in the case of heavy burden load changes.

**Keywords:** High-current clamp, DC-DC converter, Fast-response, Load regulation

## 1. Introduction

Since the beginning of the digital revolution, the speed of a microprocessor has been increased The Intel's co-founder Gorden Moore suggested that the speed of microprocessor would double in every 18 months[1] The power consumption of a high-clock-speed processor is very large because power is largely a function of frequency It can be determined by the formula P = CV2F, where P equals power, C is the capacitance of the overall system, V is voltage, and F is the operating frequency. The low voltage processes have a smaller resistor geometry that results in lower parasitic capacitance reducing the C in the above equation However, the lower output voltage higher output current, and smaller output voltage ripple requirements have greatly increased the difficulty of the power supply design Table I displays the future microprocessor power supply specifications[2] To further burden the problem, different parts in the microprocessor are turn on or off in each cycle in order to conserve power [3] It has demanded faster and more stable transient response from the DC-DC converter

Table 1 Power supply specifications of future microprocessors

| | |
|---|---|
| Input voltage | >12V |
| Output voltage | <1V |
| Output voltage regulation | <50mV |
| Load current | >350A |
| Current slew rate | >350A/us |
| Regulator response time | <200ns |

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Various modifications to the basic buck topology have been introduced to address these demanding specifications [4~14]. Reducing the output inductance of single converter may increase the output current slew rate and reduce the output voltage variation at the steep load transitions, but this method will also produce higher ripple voltage and ripple current, which is not acceptable. It is possible to parallel several converters and each converter has a relatively large output inductance. This parallel converter approach can flexibly increase output current slew rate by increasing the number of parallel converters

Interleaving parallel converter[10~12] is one special form of parallel converter configuration, which produces equivalent small output inductance. This approach can help solve the higher ripple voltage by using complicated control circuit It gives good performance during transient condition however, the steady state performance is still not satisfactory due to higher losses To solve these problems, the present paper introduces a high-current clamp, which is applied to a DC-DC converter. It provides a feature of current amplification during the fast load transient. Current is amplified during the step load transition by switching to a low inductance path. The design and the simulation of the concept are verified by experiment of 12V input and 3 3V/30A output.

## 2. Transient Analysis at Fast Load Change

An output voltage variation of a conventional buck topology (shown in Fig 1) due to sudden increase in the load current is shown in Fig 2 This output voltage variation is mainly causes the parasitic elements of the output filter capacitor It can be found in eq.1

$$\Delta V_o = \frac{1}{C_o}\int i_C\, dt + R_e \cdot i_C + L_e \frac{di_C}{dt} \qquad (1)$$

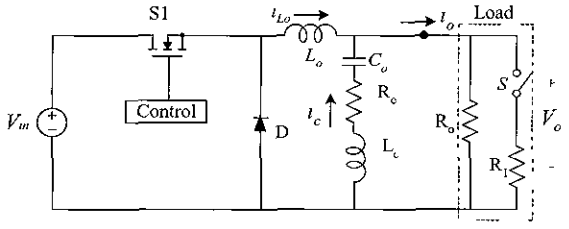



Fig 1 Conventional buck topology

During the load current transient, if load current slew rate is higher than maximum inductor current slew rate, the output current $i_o$ is partially supplied by the voltage regulator module (VRM) output filter capacitor $C_o$, until the inductor current $i_{Lo}$ reaches the load current level. The capacitor current $i_C$ shows a pulse that strongly affects output voltage ($V_o$) due to the Effective Series Resistance (ESR) and Effective Series Inductance (ESL) of the output capacitor[6]. Therefore large number of high quality capacitors in parallel are needed to meet the future requirements, it is impractical due to limited space and link impedances[7]. Furthermore, the time between the sudden steps in the load current is very short and, due to the controller delay, the controller cannot response within this short period to give regulated output voltage. So, power supply requirement for future processors are very hard to meet with the conventional buck topologies

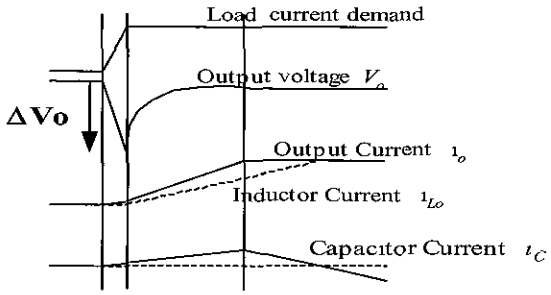



Fig 2 Transient waveforms during fast load change

The circuit parameters used in circuit analysis defined as follows

| | |
|---|---|
| Input voltage. | Vin |
| Output voltage. | Vo |
| Load current. | io |
| Inductor current at light load: | IL |
| Output capacitor: | Co |
| Effective Series Inductance (ESL): | Le |
| Effective Series Resistance (ESR): | Re |
| Switch used to change the load. | S |
| Load resistance at light load. | Ro |
| Resistance used to change the load. | R1 |
| Load resistance at light load(R1//R2):R | |

To better understand the behavior of ESR and ESL of output capacitor to output voltage variations and output To

better understand the behavior of ESR and ESL of output capacitor to output voltage variations and output current slew rate, the simplified circuit model as shown in Fig 3 is analyzed.

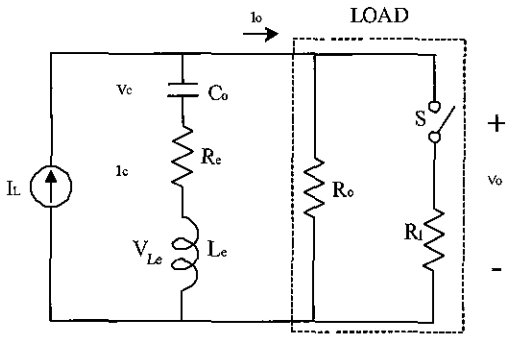



Fig 3 Simplified circuit model of buck converter

$I_L$ supposed that very slow increase at severe load change and expressed as constant current source The switch S uses for step change of load, and the load resistance ($R_l$) is on resistance of switch S. It is assumed that switch S is turn on at t=0, and derived the expressions for output current ($i_o$), output voltage ($V_o$), capacitor current ($i_c$) and voltage drop of ESL ($V_{Le}$) are in the eqs. (2),(3),(4) and (5) respectively.

$$i_o = I_L + \frac{(R_o - R)}{R + R_e} . I_L (1 - e^{-\frac{R+R_e}{L_e} t}) \quad (2)$$

$$i_c = \frac{(R_o - R)}{R + R_e} . I_L (1 - e^{-\frac{R+R_e}{L_e} t}) \quad (3)$$

$$V_o = R . I_L + R \frac{(R_o - R)}{R + R_e} . I_L (1 - e^{-\frac{R+R_e}{L_e} t}) \quad (4)$$

$$v_{Le} = (R_o - R) . I_L . e^{-\frac{R+R_e}{L_e} t} \quad (5)$$

where

$$R = \frac{(R_o R_1)}{R_o + R_1}$$

Using the above eqs.(2) to (5) output voltage under-shoot ($\Delta V_o$) at fast load change, voltage drop in recovery ($v_{drop}$) and output current slew rate ($\tau$) are derived

At fast load transition, it can be assumed t=0, output voltage under-shoot can be written as in (6)

$$\Delta V_o = (R_o - R) I_L \quad (6)$$

Voltage drop in recovery can be obtained in (7)

$$V_{drop} = \frac{(R_o - R) . R_e}{R + R_e} I_L \quad (7)$$

Also maximum output current slew rate can be found in(8)

$$\tau = \frac{(R_o - R)}{L_e} . I_L \quad (8)$$

When sudden load change occurs, the output voltage ($V_o$) and output current ($i_o$) are become wave forms as in Fig.4. And those waveforms are analyzed using the eqs. in (6),(7),(8) with three different kinds of capacitors as shown in Tab. 2. Circuit parameters are in Tab. 3. Analyzed values of output voltage under-shoot ($\Delta V_o$), voltage drop ($v_{drop}$) in recovery and output current slew rate ($\tau$) are in Tab 4

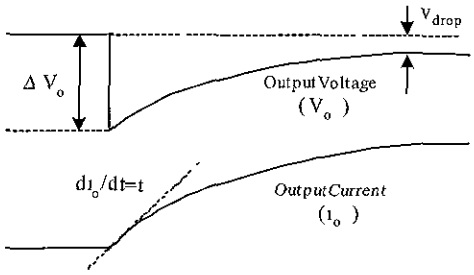



Fig. 4 Output voltage/current waveforms at fast load change

Table 2 Capacitors used in analysis

| Capacitor Type | Value (μF) | ESR (mΩ) | ESL (nH) |
|---|---|---|---|
| Electrolytic | 330 | 130 | 30 |
| OS-CON | 330 | 24 | 26 |
| CERAMIC | 330 | 8 | 18 |

Table 3 Circuit parameters.

| | | |
|---|---|---|
| Input voltage | $V_{in}$ | 12V |
| Output voltage | $V_o$ | 3 3V |
| Load resistance | Light($R_o$) | 1 0Ω |
| | Heavy($R$) | 55mΩ |
| Output filter inductor | $L_o$ | 6 3μH |
| Switching frequency | $f_s$ | 100KHz |
| Inductor Current | $I_L$ | 3 42A |

Table 4 Analyzed values of $\Delta V$, $V_{drop}$, $\tau$

| Capacitor Type | $\Delta V_o$ (V) | $V_{drop}$ (V) | τ (A/μs) |
|---|---|---|---|
| Electrolytic | 3 23 | 2 27 | 107 |
| OS-CON | 3 23 | 0 98 | 124 |
| Ceramic | 3 23 | 0 58 | 179 |

The voltage regulator module (VRM) output capacitor characteristic response to output voltage and output current is examined using three kinds of capacitors electrolytic, OS-CON, and ceramic in a fast load changes

The relation of output voltage, output current wave pattern is investigated at having applied it to a basic buck converter using C, ESR, ESL series equivalent circuit of a capacitor It realized that output voltage under-shoot ($\Delta V_o$) in a sudden load change does not depend on the types of capacitor (not depend on ESR, ESL, C) The Output voltage drop ($V_{drop}$) in recovery is depends on the ESR of the capacitor greatly

The output current slew rate (τ) is greatly depends on the ESL of the capacitor. Simulation and experiment results in Figs 5, 6 verify the analysis. Tables 5, 6 show the summary of the simulation and experiment results respectively.

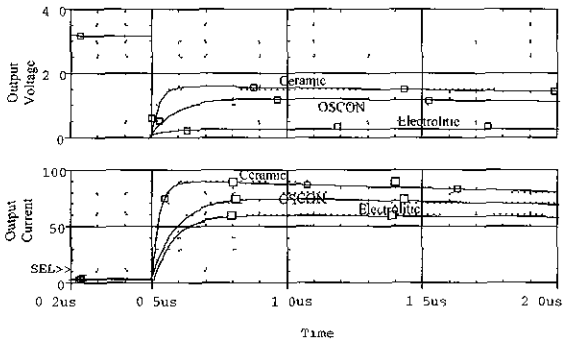



Fig 5 Simulation wave forms for three different capacitors during the fast load change.

Table 5 Simulation results of $\Delta V$, $V_{drop}$, $\tau$

| Capacitor Type | $\Delta V_o$ (V) | $V_{drop}$ (V) | τ (A/μs) |
|---|---|---|---|
| Electrolytic | 3 24 | 3 0 | 15 |
| OS-CON | 3 24 | 2 0 | 77 |
| Ceramic | 3 24 | 1 4 | 96 |

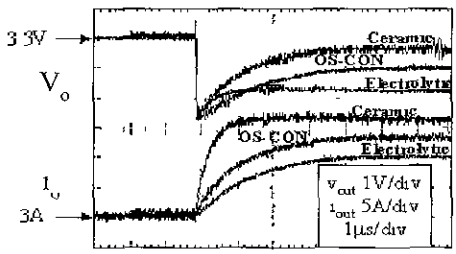



Fig 6 Experiment wave forms for three different capacitors during the fast load change.

Table 6 Experiment results of $\Delta V$, $V_{drop}$, $\tau$

| Capacitor Type | $\Delta V_o$ (V) | $V_{drop}$ (V) | τ (A/μs) |
|---|---|---|---|
| Electrolytic | 2 84 | 2 0 | 15 |
| OS-CON | 2.84 | 1 0 | 67 |
| Ceramic | 2 84 | 0 4 | 86 |

## 3. Proposed Solution

### 3.1 Circuit Description

The high-current clamp technique is simple system to improve the transient response during the fast load transitions. As shown in Fig. 7, high current clamp is theoretically loss less, low cost and easy to implement with simple control scheme This is modified from a basic buck topology by replacing the output inductor with two magnetically coupled inductors Inductors are difference in inductance, one has large inductance (Lo) and the other has small inductance (Ls) The inductor with small inductance will take over the output inductor during step load transient It speedup the output current slew rate and reduce the output voltage drop The diode $D_s$ is prevents the reverse current flow at the step-up load transition. Very low on resistance schottky rectifier is used as $D_s$ to minimize the losses

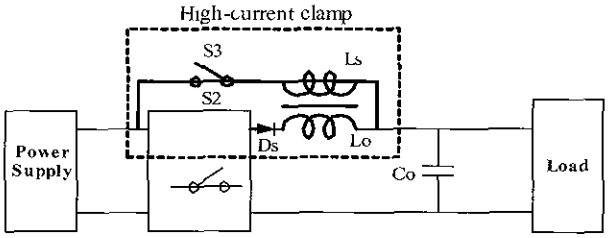



Fig 7 Block diagram of proposed DC-DC converter

### 3.2 Analysis of High-Current Clamp Response

Figure 8 shows the complete circuit diagram of proposed converter with high-current clamp which is applied to the basic buck topology The circuit can be analyzed with considering the fast load change of step-up load transition Ideal characteristic of coupled inductor is assumed for the analysis.

The sub-switch S2 in Fig. 8 is activated only in case of large current variation at the steep load transition The output voltage (Vo), drops below a certain reference level, switch S2 is turned on by the control signal (Ctrl1) and the small inductor (Ls) takes over the output inductor This makes the very low inductance path and large current flows through the inductor (Ls). High current through the smaller inductor (Ls), increases the load current slew rate and reduce the output voltage under-shoot. There exist two states of main switch (S1) at this transition

### State1: Switch S1 ON, S2 ON

The eqs (9-12) can be written from the Fig. 9(a) and it shows the state1 at t=0. Finally, condition (13) is derived According to the eq.(13), the diode (Ds) is reverse bias and resulting equivalent circuit is as in Fig 9(b) Therefore, it makes sure the only small inductor (Ls) is conducting to make the high current path during the steep load change.

$$V_{Ls} = (V_{in} - V_o) \tag{9}$$

$$V_{Lo} = \frac{n_1}{n_2}(V_{in} - V_o) \tag{10}$$

$$V_{Lo} > V_{Ls} \because (n_1 > n_2) \tag{11}$$

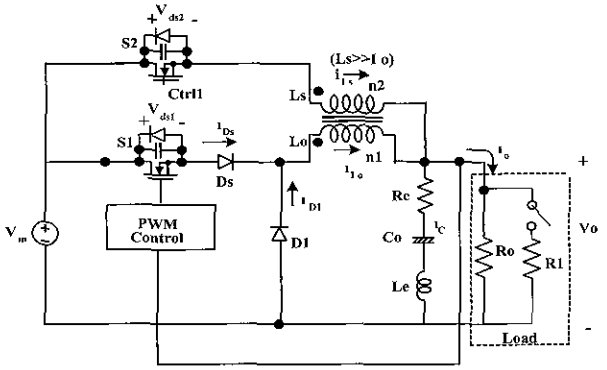


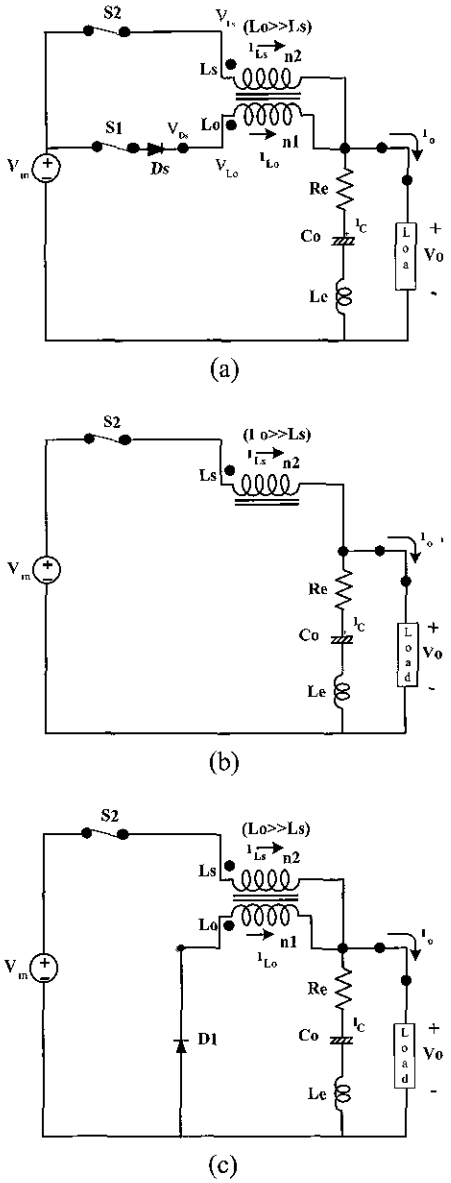

Fig 8 Complete circuit diagram of proposed DC-DC converter

$$V_{Lo} = V_{Ds} - V_o \tag{12}$$

$$V_{Ds} > V_{in} \tag{13}$$

### State2: Switch S1 OFF, S2 ON

Figure 9(c) shows the state2 In this state, the diode (D1) is reverse bias and resulting equivalent circuit is same as Fig 9(b) and only inductor (Ls) is conducting to make the high current path.




(a) circuit at state1 (t=0), (b) circuit at state1 (t>0), (c) circuit at state 2

Fig 9 Simplified circuit during steep load transition

It is realized that, the small inductor Ls (<<Lo) takes over the output inductor of the converter during the step-up load transition High current through the small inductor (Ls) increases the load current slew rate and reduce the output voltage under-shoot. Therefore, proposed circuit can be considered as buck converter with very small inductance at fast load transition

From eq.(1), the output voltage variation can be expressed as in eq (14)

$$\Delta V_o = \frac{1}{C_o}.\int(i_o - i_{Lo}).dt + R_e\, i_C + L_e.\left(\frac{di_C}{dt}\right) \tag{14}$$

According to the eq (6) in section 2, the out put voltage under-shoot at fast-load change is not depends on the ESR and ESL of the output capacitor, therefore eq (14) can be reduced to eq (15)

$$\Delta V_o = \frac{1}{C_o}\int(i_o - i_{Lo})dt \tag{15}$$

From eq (15), output voltage under-shoot without high-current clamp ($\Delta V_{woc}$) is

$$\Delta V_{woc} = \frac{1}{C_o}\int(i_o - i_{Lo})dt \tag{16}$$

Using the eq.(15) reference to the Fig 9(b) output voltage drop with high-current clamp ($\Delta V_{wc}$) can be expressed as follows;

$$\Delta V_{wc} = \frac{1}{C_o}\int(i_o - i_{Ls})dt \tag{17}$$

From the Fig 9(a), $i_{Ls}$ can be expressed as in eq. (18)

$$i_{Ls} = \frac{n1}{n2}.i_{Lo} \tag{18}$$

substitute $i_{Ls}$ to eq (17);

$$\Delta V_{wc} = \frac{1}{C_o}\int(i_o - \frac{n1}{n2}\, i_{Lo})dt \tag{19}$$

from eq.(16) and eq.(19), following argument can be obtained,

$$\Delta V_{wc} << \Delta V_{woc} \tag{20}$$

where $n1>>n2$

From the eq (8) load current slew can be written for both cases of conventional (without clamp) and proposed (with clamp),

$$\tau_{woc} = \frac{(R_o - R)}{L_e}.I_{Lo} \tag{21}$$

$$\tau_{wc} = \frac{(R_o - R)}{L_e}\, I_{Ls} \tag{22}$$

substitute from eq (18),

$$\tau_{wc} = \frac{(R_o - R)}{L_e}\,\frac{n1}{n2}.I_{Lo} \tag{23}$$

from eqs.(21) and (23), following expression can be obtained,

$$\tau_{wc} = \frac{n1}{n2}.\tau_{woc} \tag{24}$$

where $n1>>n2$

The eqs. (20) and (24), show that the output voltage under-shoot is reduced and output current slew rate is increased with proposed topology during the fast load change Figure 10 shows the compensation of high-current clamp

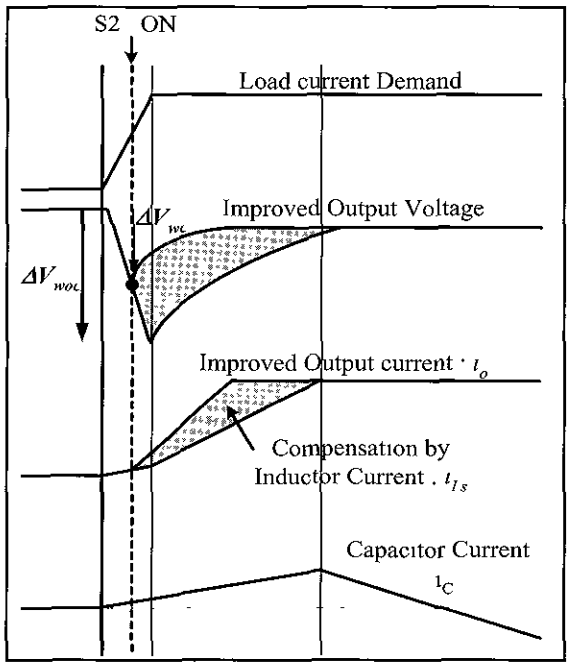



Fig 10 Compensation of high-current clamp

### 3.3 Steady state operation:

In steady state, only the large inductor Ls takes over the output inductor and keeps the substantially small-ripple current. Output ripple can be designed to be small as possible using large steady state output inductor is an advantage. Steady state performance is equivalent to today`s sophisticated buck converter and practically very little power loss due to transient operation.

### 3.4 Control Method:

An additional comparator is used to control the switch related to step load transition. In the case of sudden load current variation, the output voltage below certain reference level the switch S2 is turned-on by the control signal (Ctrl1) to make the high current path while connecting the small inductor to the main circuit. Figure 11 shows the control scheme.

This simple control method provides the substantial constant output voltage in the case of severe load changes. This can be implemented with existing PWM controller IC.

The extra cost and design effort for such improvement is minimized as only low cost small size components are needed.

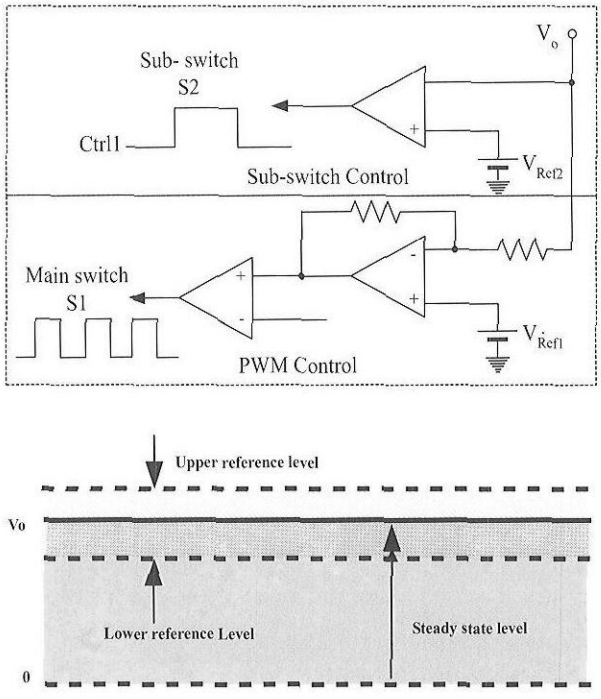



Fig. 11. Control scheme

## 4. Implementation

Based on the specification and components in the table 7, the simulation is performed using the OrCAD software. In order to verify the results, the experimental circuit is built for a 12V to 3.3V/30A voltage regulator module as shown in Fig.8.

### 4.1 Simulation Results

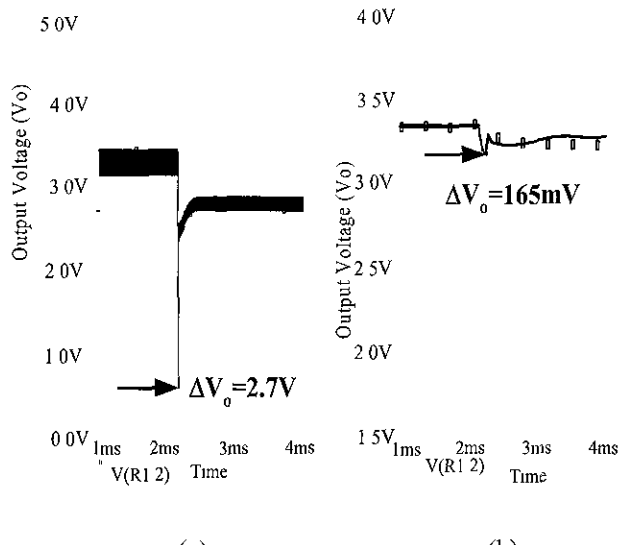
Figures. 12(a), 12(b) show the simulation results of the dynamic response of the converter specified in Table VII, without and with the high-current clamp respectively. According to the simulation results the output voltage variations for the conventional topology is 2.7V and the proposed topology is 165mV during the steep load transition

### 4.2 Experiment Results

Experimental circuit is build with the specifications and components in the table 7. Experiment results in the Figs. 13(a), 13(b) show that the output voltage variation during the steep load transition is 2.9V for the conventional buck topology without clamp. 176mV for the proposed topology. Both experiment and simulation results are almost close with little differences due to conduction losses.

Table 7. Specifications and circuit parameters.

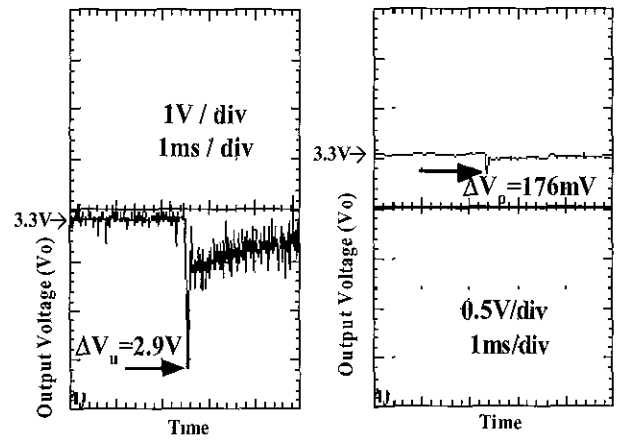
| | | |
|---|---|---|
| $V_{in}$ | Input voltage | 12V |
| $V_o$ | Output voltage | 3.3V |
| $R_o$ | Light load (1A) | 3.3Ω |
| $R$ | Heavy load (30A) | 0.11mΩ |
| $L_o$ | Output filter inductor | 6.3μH |
| $Ls$ | Small inductor | 100nH |
| $f_s$ | Switching frequency | 100KHz |
| $I_L$ | Load current slew rate | 150A/μS |
| $Co$ | Output capacitor | 330μF |
| $Re$ | ESR of output capacitor | 130mΩ |
| $Le$ | ESL of output capacitor | 30nH |




(a) (b)

(a) Conventional topology,
(b) Proposed topology (Load change from 1A to 30A)

Fig 12 Simulation results Output voltage variation during steep load change




(a) (b)

Fig 13 Experiment results Output voltage variation during steep load change,(a) Conventional topology ,(b) Proposed topology (Load change from 1A to 30A)

### 4.3 Converter Efficiency

Steady state performance is equivalent to today's sophisticated buck converter, and practically very little power loss due to diodes D1, Ds. However, using the large steady state output inductor, output ripple can be designed to be very small Also very low on resistance schottky rectifiers are used to minimize the losses If compared with the conventional topologies proposed topology involves power losses during transients due to the activation of the low inductance high current path. It is slightly affect the efficiency of whole converter system. According to the Fig 14, for the conventional topology efficiency is 83% at 30A The introducing a high-current clamp it is reduced by 1 1%, a largely acceptable for the real applications reference to the standard voltage regulator module (VRM) design guidelines [15].

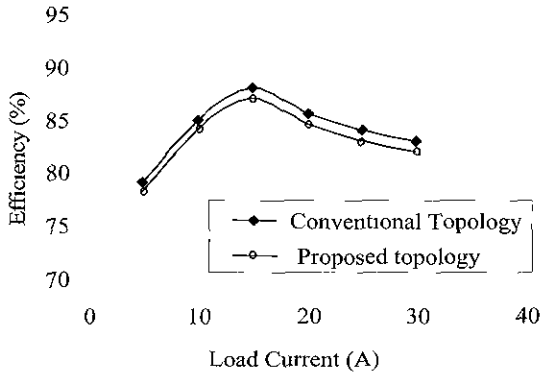



Fig 14 Efficiency comparison

## 5. Conclusions

The basic design of the DC-DC converter with high-current clamp has been proposed and experimentally verified. Both simulation and experimental results prove that proposed topology is improved the transient response significantly during the steep load transitions The output voltage under-shoot at the step load transition is 5% ($\Delta V_o$=176mV) The proposed converter can be applied to conventional buck converter much improve transient response with only an additional MOSFET and a diode. Control circuit is simple and can be implemented with an existing PWM controller IC. Also in steady state, output ripple can be designed to be small as possible using large steady state output inductor It is believed that the proposed topology is very suitable for fast transient response requirement of present and future micropro -cessors in a compact size at a very affordable price

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## References


[1] G.Moore, "Progress in digital integrated electronics," *International Electron Device Meeting Tech. digest,* 1975, pp. 11-13.

[2] B.Rose, "Voltage Regulator technology requirements," *4th Annual Intel Technology Symposium,* USA, Sept. 2000.

[3] Andrew.J.Burstein, "Voltage regulation using an estimated current", *US Patent* No. 6, 031, 361, Feb. 2000.

[4] Albert M. Wu, etc.., "An active clamp circuit for voltage regulation module(VRM) applications," *IEEE Transac tions on Power Electronics*, Vol. 16, No. 5, pp. 623-634, Sep. 2001.

[5] Xunwei,etc.., "Investigation of candidate VRM topology for future microprocessors", *VPEC Seminar,* pp. 9-14, Sept. 1997.

[6] A.Consoli,A.Tesla,G.Giannetto,F.Gennaro, "A New VRM Topology for Next Generation Microprocessors", *PESC Record,* pp. 339-344, June. 2001.

[7] Pit-Leong Wong,Xunwei Zhou,Jiabin Chen,Ho-Pu Wu,Luca Amoroso,Jiangang Liu,Fred C.Lee,Xingzhu Zhang and Dan Y.Chen , "VRM transient study and output filter design for future processor,"*VPEC Seminar,* pp. 1-7, Sept. 1997.

[8] Wei Chen,Fred C.Lee,Xunwei Zhou and Peng Xu, "Intergrated Planar Inductor Scheme for Multi-module Interleaved Quasi-Square-Ware(QSW) DC/DC Converter", *VPEC Seminar*, pp. 17-21, Sept. 1998.

[9] Luca Amoroso, Mauro Donati, Xunwei Zhou and Fred C.Lee, "Single shot transient suppressor for high slew rate microprocessors", *APEC Record,* pp. 284-288, Mar. 1999.

[10] Peng Xu,Yuan-chen Ren,Mao Ye and Fred C. Lee, "A family of Novel Interleaved DC/DC Converters for Low-Voltage High-Current Voltage Regulator Module Applications", *PESC Record 2001*, pp. 1507-1511.

[11] M.T Zhang,M.M Jovanovic and F.C.Y. Lee, "Analysis and Evaluation of Interleaving Techniques in Forward Converters", *IEEE Transactions on Power Electronics*, Vol. 13, No. 4, 1998, pp. 690-698.

[12] Pit-Leong Qiaoqiao Wu, Peng Xu, Bo Yang and Fred C.Lee, "Investigating coupling inductors in the interleaving QSW VRM", *APEC Record, 2000*, pp. 973-978.

[13] T.Senanayake,T.Ninomiya, "Improvement of Inductor-Switching DC-DC Converter for Fast-Response VRM", IEEE-Kyushu Chapter Convention Conference in Power Electronics, pp. 26-27, Sept. 2002.

[14] T.Senanayake, T.Ninomiya, "Fast-Response Load Regula tion of DC-DC Converter By Inductor-Switching High Current Path," *IEEE TENCON 2002*, pp. 1986-1989. Oct. 2002.

[15] Intel "VRM 9.0 DC-DC converter design guidelines", Apr. 2002.


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